SPARCstation™ 10 System Architecture

Technical White Paper

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Contents

Introduction

The SPARCstation™ 10 system is a new milestone in Sun's vision for the next generation of desktop workstation computing. A new design from the ground-up, the SPARCstation 10 delivers several breakthroughs in the areas of CPU, memory, graphics, and input/output technology.

The first desktop workstation to incorporate symmetrical multiprocessing, the SPARCstation 10 is designed to deliver system throughput up to several hundred SPECs.

The SPARCstation 10 system CPU is fully upgradable to the next generation of even faster SPARC® CPU technology since the CPU is packaged on a plug-in, standardized MBus module. This eables the end user to preserve their system investment.

The SPARCstation 10 system provides very large memory capacity to allow the user to run very large applications at high speed. This ECC memory has a maximum capacity of 512 Mbytes and is accessed at high speed through a 144-bit wide memory data path.

The SPARCstation 10 system includes a number of new standard motherboard input/output functions compared with its predecessors. It features ISDN, twisted-pair Ethernet, 10 Mbyte per second SCSI, a parallel port, and a 16-bit stereo audio system that is packaged in an external speaker box. In addition, there are four SBus slots for I/O expansion. Maximum internal disk storage is 2 Gbytes, externally expandable to over 50 Gbytes.

With all this functionality, the SPARCstation 10 system still fits in the “pizza box” form factor pioneered by Sun with the SPARCstation 1 system in 1989. This compact form factor required highly integrated electronics, a new power supply, and a way of cooling developed specifically for this product.

The SPARCstation 10 system comes with the Solaris® 1.1 operating system and thus remains binary compatible with the installed base of over 500,000 SPARCstations worldwide.

System Overview 1

The SPARCstation 10 system is the most recent addition to the Sun™ family of desktop SPARC computers. Like its predecessors, the SPARCstation 10 system shares a number of common features, including conformance to the SPARC architecture, the SBus, and a pizza box package. Unlike its predecessors, however, the SPARCstation 10 system has several new features which, as a system, bring important new functionality to the desktop. These include a new superscalar SPARC processor, symmetric multiprocessing, upgradable processors, and ISDN.

The purpose of this paper is to provide the reader with an overall feel for the features, functionality, and architecture of the SPARCstation 10 system. A set of companion papers discuss the particular details of the system, such as Sun's new SuperSPARC™ processor, in much greater detail.

Historical Perspective

SPARCstation 1, the first desktop SPARCstation, was introduced in April of 1989. Also in the SPARCstation 1 family are the SPARCstation IPC system, the SPARCstation SLC system, and the SPARCstation 1+ system, which were introduced in early 1990. As shown in Table 1, the SPARCstation 1 performs at 9.6/7.8 (SPECint92/SPECfp92). Beginning in the fall of 1990, Sun introduced its second family of desktop workstations based on the Sun-4c architecture: the SPARCstation 2, the SPARCstation IPX, and the SPARCstation ELC. These machines deliver SPEC92 performance of up to 22.4/22.6. The SPARCstation 10 implements the new Sun-4m architecture to achieve new levels of performance with SPEC92 ratings that range from 44.2/52.9 for the Model 30, 52.6/64.7 for the Model 41 and up to 8 times the performance of a SPARCstation 2 with the 2 multiprocessing CPU configurations.

Perhaps the single most important feature of the SPARCstation 10 system is that it is application software-compatible with its predecessors. Application binaries that run on the more than 500,000 SPARCstation systems already installed, run unmodified on a SPARCstation 10 system running Solaris 1.1 (SunOS™ 4.1.3).

Table 1-1 Desktop SPARCstation Family Comparison[1]

Feature	**SPARCstation 1**	**SPARCstation 2**	**SPARCstation 10 Model 30**	**SPARCstation 10 Model 41**	**SPARCstation 10 Model 52**	**SPARCstation 10 Model 54**
Introduced	April 1989	November 1990	May 1992	May 1992	May 1992	May 1992
Processor	SPARC	SPARC	SPARC	SPARC	SPARC	SPARC
Semiconductor Partners	Fujitsu MB86901A LSI Logic L64801	Cypress CY7C601 Weitek WTL8601	TI TMS390Z50	TI TMS390Z50	TI TMS390Z50	TI TMS390Z50
Clock Speed	20 MHz	40 MHz	36 MHz	40 MHz	45 MHz	45 MHz
SPECint92	9.6	22.4	44.2	52.6	N/A[2]	N/A[2]
SPECfp92	7.8	22.6	52.9	64.7	N/A[2]	N/A[2]
SPECthruput89	N/A	N/A	N/A	N/A	109	218
MIPS	12	25	86.1	96.2	200+[3]	400+[3]
MFLOPS (DP)	2.5	4	10.6	17.2	38[3]	76[3]
Cache Size	64 KB	64 KB	36 KB	36 KB + 1 MB	2 x (36 KB + 1 MB)	4 x (36 KB + 1 MB)
Max. Memory	64 MB	128 MB	512 MB	512 MB	512 MB	512 MB
Max. Intern. Disk	200 MB	400 MB	2 GB	2 GB	2 GB	2 GB
I/O Bus	SBus	SBus	SBus	SBus	SBus	SBus
Chip Count[4]	50	41	34	34	34	34

1. Benchmarks are run using Solaris 1.1, and a combination of Apogee/KAP and SunPro/KAP compilers. 2. No MP SPEC92 definition exists at this time for multiprocessors so SPECthruput89 estimates are provided below. 3. MP system performance numbers are estimates. 4. Logic chips on main logic board.

System Overview

Compared with its predecessors, the SPARCstation 10 system offers considerably more expandability. It offers significantly improved uniprocessor performance, multiprocessing capability (up to 4 CPUs on the desktop), more DRAM memory (512 Mbytes), more bandwidth (up to 320 Mbytes per second for memory and I/O), more SBus slots (4), more internal disk storage (up to 2.0 Gbytes), and more connectivity (TP Ethernet, ISDN, a Centronics-compatible parallel port, digital audio port) than ever before. Equally important, it has the same footprint and overall dimensions as the original SPARCstation "pizza-box" design, yet due to a new power-supply design and an improved package, it is actually quieter.

Figure 1-2 shows the inside of a SPARCstation 10 system. Like its predecessors, the SPARCstation 10 system enclosure includes a power supply, a DOS-compatible floppy disk, two hard disk drives, and a single-board computer. The SPARCstation 10 system has only five screws: one to hold the top cover in place, two to hold the backpanel on, and two to hold the CPU board in place. To make the system more reliable and easier to upgrade and service, the base of the machine is now made out of plastic, instead of sheet metal. As a result, some plastic features were added to the case, such as disk drive and motherboard brackets, to make removing and installing these components much easier. At the same time, the all-plastic enclosure allows for a double-stacked processor and I/O board configuration, which greatly increases the expandability of the system. Finally, this enclosure with its modified industrial design of the top cover, significantly increases the airflow through the system, allowing for an overall power dissipation of 140W with noise of only 4.7 Bels. This is in contrast with the earlier generation of Sun machines that had a power dissipation of 85W, yet a noise level of 5.3 Bels. This is possible because the three variable speed fans on the SPARCstation 10 system's power supply are tied to the temperature gradient inside the package.

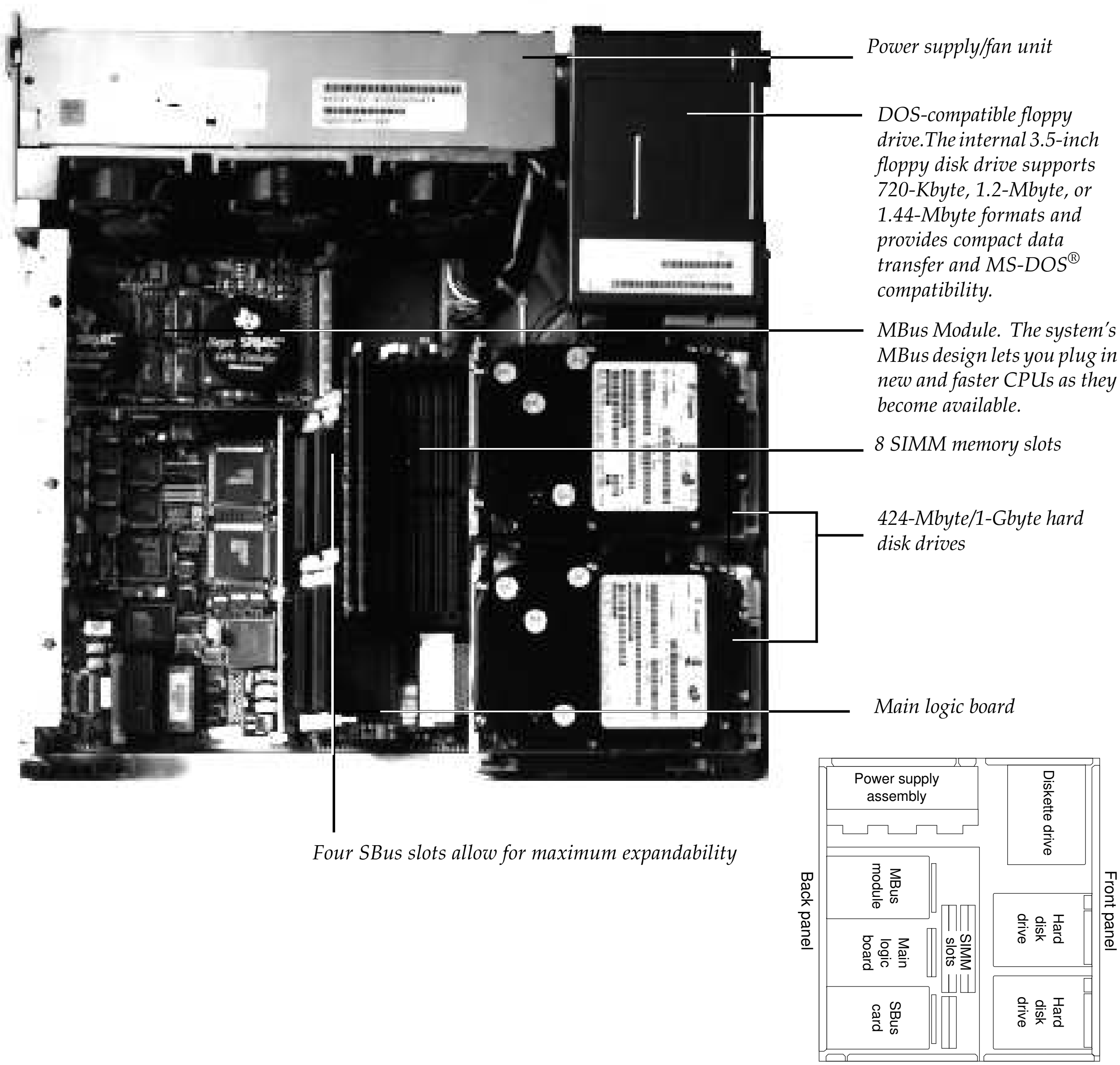


Figure 1-1 Interior of a SPARCstation 10 system

The Sun-4c architecture implemented in the SPARCstation 1 and SPARCstation 2 systems and the Sun-4m architecture implemented in the SPARCstation 10 system are distinctly different. The key difference between the two systems is that Sun-4c machines use a single combined memory and I/O bus, versus a split bus architecture of Sun-4m machines. Another major difference is that the SPARCstation 10 system's Sun-4m architecture supports symmetric multiprocessing and substantially improved memory and I/O bandwidth. The Sun-4m architecture specification is intended to be a generic architecture for all Sun Workstations® and servers so that CPUs, ASICs, and software can be leveraged across several platforms. Figure 1-2 is a block diagram of the Sun-4m architecture.

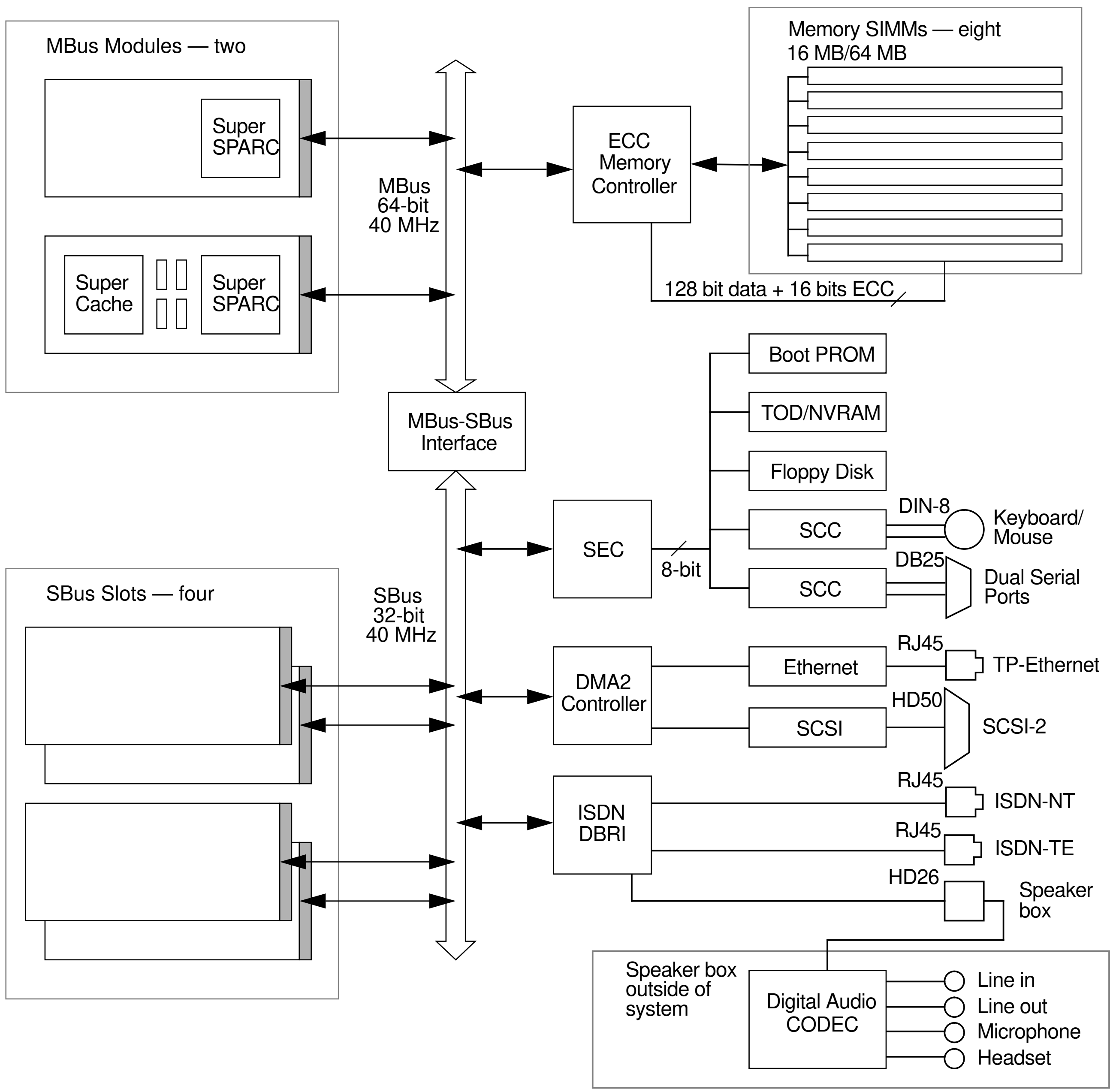


Figure 1-2 Sun-4m architecture used in the SPARCstation 10 system.

Figure 1-3 shows a photograph of the actual CPU board. Conversations with key customers and users of earlier SPARCstation systems prior to and during the development of SPARCstation 10 system revealed that besides performance, expandability and configurability were probably the two biggest issues. In designing the SPARCstation 10 system motherboard, Sun developed several new connectors that allowed SPARCstation 10 system to have additional SBus slots, a much wider data path, field upgradable processor modules, and several new I/O devices with backpanel connections. Indeed, the effort spent in designing connectors was the equivalent of the effort spent designing new ASICS.

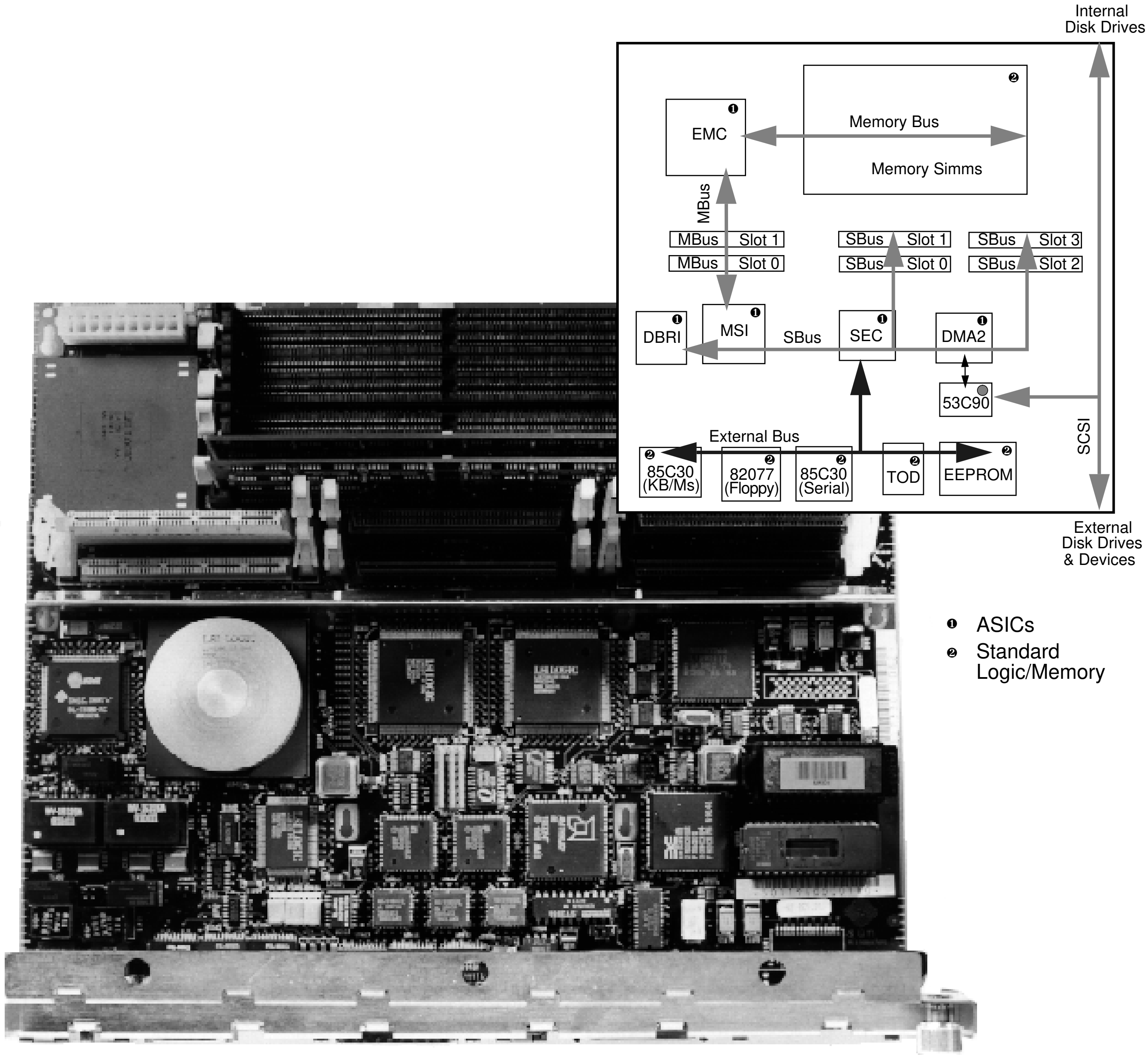


Figure 1-3 SPARCstation 10 system CPU Board

Architectural Features 2

The SPARCstation 10 system's Sun-4m architecture has the following major subsystems and architectural components:

- New SPARC modules featuring the SuperSPARC processor (discussed elsewhere in this paper).
- The MBus, which is a high-performance cache-coherent multiprocessor interconnect.
- A new main memory architecture featuring 144-bit wide SIMMs with built-in automatic single-bit correcting, double-bit detecting code.
- Improved I/O interconnect structure.

SPARC Modules

A SPARC MBus module typically includes the following (logical) components:

- A SPARC IU.
- A SPARC FPU.
- A SPARC Reference MMU.
- A cache controller with tags. Multiprocessor systems generally include two sets of tags, in order to support cache-coherence.
- Cache data RAMs.
- MBus interface.

Several of the SPARC CPU cores combine the cache, the MMU, the tags, and the MBus interface onto a single chip called the MCT but have external cache RAMs. The SuperSPARC controller merges the MCT, the data RAMs, the IU, and the FPU into a single microprocessor chip.

Most MBus machines use SPARC processors, though the system architecture allows other architecture of CPUs (for example, 80x86, 680x0) to be plugged into the system with a suitable processor bus to MBus interface chip. Indeed, the MBus specification is an open specification under the control of SPARC International, and available to all developers.

The SuperSPARC Microprocessor and System Performance

The MBus processor module concept enables the SPARCstation 10 system to support a variety of processor configurations. All processor modules currently available with the SPARCstation 10 system are based on the SuperSPARC microprocessor, a single high-performance CPU chip that is discussed in detail in a companion paper. Major features of the SuperSPARC microprocessor are:

- A single chip with integer, floating point, memory management, and caches.
- Superscalar pipeline with up to three instructions launched per clock cycle.
- 16-Kbyte instruction cache and 20-Kbyte data cache.
- 64 entry TLB with hardware page-table walking.
- Support for 65,536 contexts.
- Integral support for cache-coherent multiprocessing.
- 3.1 million transistor processor implemented using 0.8 micron BiCMOS process technology.

A companion chip, the SuperCache controller, provides for a 1-Mbyte external cache. In addition, the SuperCache controller has a phase locked-loop clock synchronization circuit so SPARC modules with SuperCache controllers can operate asynchronous to the system clock. This means that customers can take advantage of the latest advances in processor designs simply by plugging SPARC modules that clock 50, 60, 70, and higher MHz, into the 40 MHz MBus slots.

Two types of SPARC modules are used on the SPARCstation 10 system, one type running at 40 and 45 MHz:

- 36-MHz SPARC module with no external cache
- 40 MHz SPARC module with the SuperCache controller and 1 megabyte of external cache.
- 45 MHz SPARC module with the SuperCache controller and 1 megabyte of external cache.

Multiprocessor versions of the SPARCstation 10 system use two of the 45-MHz SPARC modules.

SPARC Reference MMU

A key feature of the SuperSPARC CPU is the incorporation of the SPARC Reference MMU (SRMMU) memory management scheme. The SRMMU performs two principal functions:

- Address translation from virtual to physical addresses of each running process to physical address in main memory
- Access protection, preventing a process from reading or writing the address space of another process without permission

In contrast to previous desktop systems, which used high-speed lookup tables managed and loaded by the operating system, processors in the SPARCstation 10 system use a hardware-managed translation-lookaside buffer (TLB). This approach eliminates the slow and expensive process of using software to load the lookup tables into static RAM memory. Although applications can still "thrash" the TLB by having wildly erratic memory references to a large number of pages, the SRMMU architecture offers a significant performance boost for most applications. It provides quick response times even in heavy multiuser environments, and performs especially well in database applications.

Important features of the SRMMU are:

- 4-Kbyte pages.
- 4-level translation hierarchy: contexts regions, segments, pages.
- 256 contexts, 256 regions, 64 segments.
- 32-bit (4-Gbyte) virtual address within a context.

The MBus

A major architectural innovation in the SPARCstation 10 system is a high-performance memory bus, called the MBus, which was first introduced in Sun's SPARCserver™ 600MP family. The MBus is the backbone of the machine. The overall technical features of the bus are summarized in Table 2-3. From a functional perspective the MBus has four principal attributes:

- Field-installable processor modules.
- Support for symmetric multiprocessing.
- High-bandwidth access to memory and I/O.
- Not Sun proprietary.

Field-installable processor modules. In previous systems, a new system motherboard was required to upgrade the system. Upgrading a SPARCstation 10 system, however, is as simple as either adding a processor module (to turn a uniprocessor into a multiprocessor) or upgrading a slower processor module with a higher-performance module (for example, changing from a processor without external cache to one with external cache). Supporting field-installable processor modules required special attention to both the physical and electrical design of the bus. A special connector was designed to help maintain the overall electrical impedance. The bus travels less than four inches across the PCB board and has a maximum of 6 electrical loads.

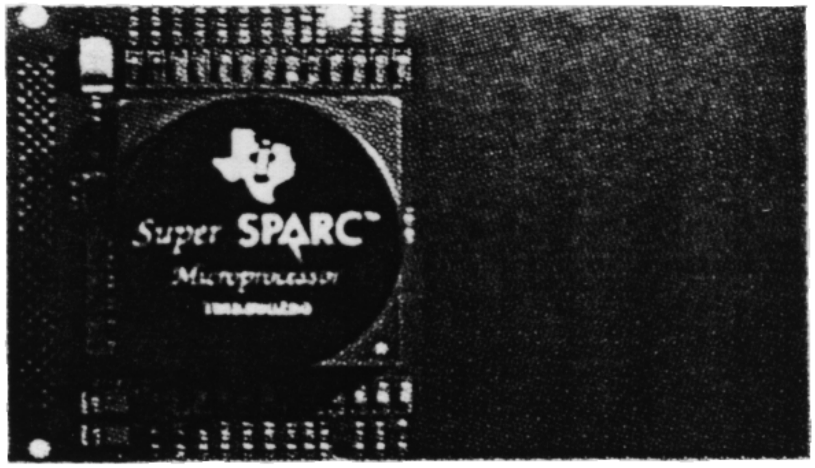
Symmetric multiprocessing. The MBus supports cache coherent multiprocessing by means of a "snooping"' protocol. Whenever a processor puts an address onto the MBus, all other processors "snoop" the bus, checking to see if data at the snooped address is in their cache. Depending on the kind of transaction, the various caches on the bus may either supply the data, mark it as shared, and/or invalidate it.

High-bandwidth. The MBus is a synchronous, 40-MHz 64-bit bus that is capable of a peak transfer rate of 320 Mbytes/second. For typical 32-byte cache fills, it can sustain roughly 100 Mbytes/second. Besides contributing to CPU performance by quickly filling the cache, another important benefit of this architecture is that even when the SBus is performing data transfers at peak transfer rates, there is still significant bandwidth available to the CPU. This is in contrast to earlier SPARCstation systems, where it was possible for the I/O to significantly reduce processor performance by using all the memory bandwidth. One of the principal motivations for providing such high-bandwidth is to support high-bandwidth I/O devices such as real-time video.

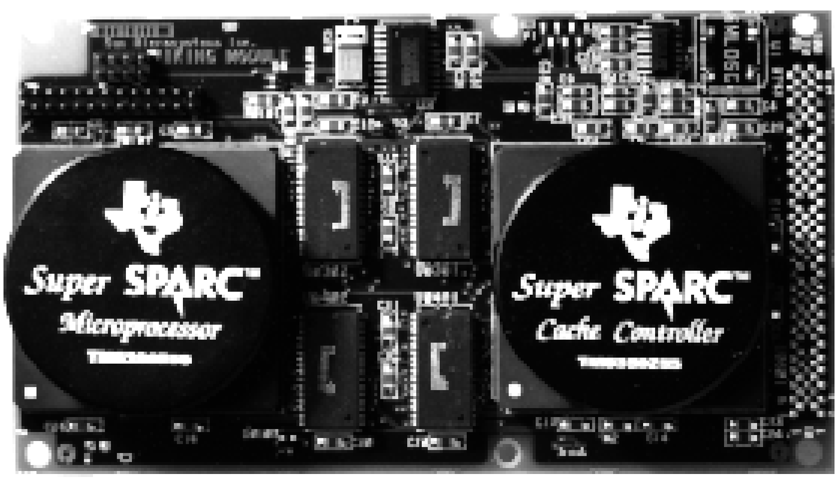
Nonproprietary. The final key aspect of the MBus is that it is nonproprietary. All rights to the bus are held by SPARC International, an independent industry organization. Thus, all vendors of SPARC chips, and third-party developers of support components are free to develop silicon that interfaces to the Bus. To date, a wide variety of companies, including Texas Instruments, LSI Logic, and Ross Technologies (a Cypress Semiconductors subsidiary), have developed processors and chips to interface to the MBus.

Table 2-1 Basic MBus Features

Feature	
Clock Speed:	40 MHz
Total Signals:	100
Style:	Synchronous, multiplexed address/data
Data-width:	64 bits
Address:	36 bits, physical address
Coherency protocol:	Snooping with ownership/invalidate
Peak data rate:	320 Mbytes/second
Sustained bandwidth:	100 Mbytes/second
Maximum number of processors:	4 (2 processor modules with 2 processors each)



SuperSPARC module without external cache



SuperSPARC module with 1 megabyte of external cache

Figure 2-1 MBus modules

The MBus, Cache Coherency, and Multiprocessing

The MBus is a specification for interfacing CPU modules to memory and, ultimately, to I/O. Because the MBus runs at 40 MHz, it is not as easy to interface to as the SBus and greater care is required in the electrical design of the boards and chips that comprise the MBus. Another distinction between the MBus and the SBus is that the SBus supports virtual addressing by DVMA masters, while the MBus is a physically addressable bus.

The MBus supports hardware cache-coherence and multiprocessing. Systems that don't support cache coherence are called Level 1 MBus machines; those that do are Level 2 MBus machines. Support for the MBus Level 2 protocols is required by all MBus participants: CPU modules, memory, and I/O interfaces. Hardware cache coherence is useful for multiprocessing and for I/O because it avoids software flushing of processor caches, which can cause significant CPU overhead on SPARCstation 1 and SPARCstation 2 systems.

The SPARCstation 10 system motherboards are Level 2 compliant. This means the memory subsystem and the MBus-to-SBus interface supports Level 2 MBus protocols. However, the level of a particular SPARCstation 10 system depends on the CPU module plugged into the system. Some CPU chip sets are Level 1 compliant; others, like the SuperSPARC microprocessor, are Level 2 compliant. If a Level 1 processor module is plugged into the system, it will be a Level 1 machine even though the motherboard supports Level 2. Operating system software in this case must perform a cache flushing. If a Level 2 processor is plugged into a SPARCstation 10 system, then the whole system can be cache coherent, assuming that the operating system chooses to take advantage of the processor.

Note – A Level 1 operating system will work in a single-processor Level 2 system.

Main memory Architecture

In both Sun-4m and Sun-4c machines, the main memory of the system interfaces to the processor bus through a memory controller. In earlier machines, memory was 36 bits wide, with 32 bits of data and 4 bits for byte parity. In order to meet the bandwidth requirements of the SPARCstation 10 system, a much wider memory system with 144 bits total (128 bits of data and 16 bits of error detection and correction) necessary. As shown in the block diagram, the memory subsystem consists of a single-chip memory controller and eight 200-pin custom SIMM modules, as shown in Figure 2-2. The SIMM modules take advantage of new memory packages, which enable memory chips to be mounted on both sides of the board. In addition, a special dual-readout SIMM socket developed for the SPARCstation 10 system, enables double the signal density found in typical SIMM sockets. A special ejector lever was included as part of the connector design to facilitate removal.

There are two important advantages of the 128-bit wide memory data path. The first is that a 32-byte cache fill can be accomplished quickly. The second is that error correction can be performed on each 64-bit word. The error correction scheme used in the SPARCstation 10 system corrects any single bit error, and will detect any double-bit or nibble (4-bit) error. The nibble detection is quite valuable, as the DRAM chips used are 4 bits wide. Thus, the failure of an entire DRAM chip can be detected.

As shown in Figure 2-2, two types of memory SIMMS can be inserted into the 8 SIMM slots: a 16-Mbyte SIMM constructed using 4-Mbit DRAMS, and a 64-Mbyte SIMM constructed using 16-Mbit DRAMS. The 8-SIMM sockets provide a maximum memory of 128 Mbytes with 4-Mbit SIMMs and 512 Mbytes with 16-Mbit SIMMs. 4- and 16-Mbit SIMMs may be mixed and matched and will be automatically configured by the system without setting of jumpers.

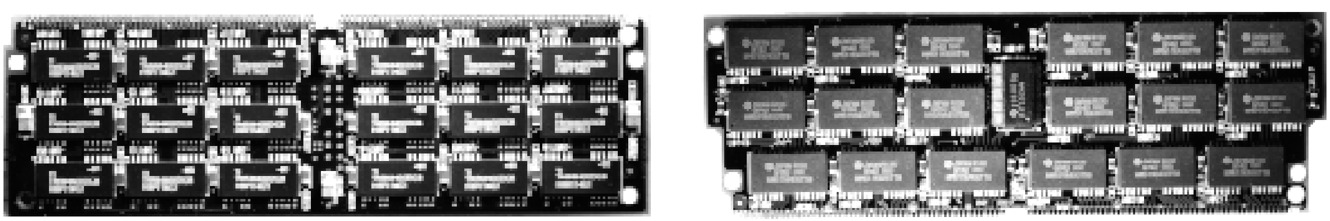


Figure 2-2 SPARCstation 10 system memory SIMMs

I/O Architecture

Unlike earlier desktop machines where the SBus was used for both I/O and system memory, in the SPARCstation 10 system the memory and I/O bus are independent. The MBus is used as the processor memory interconnect, while the SBus is used *only* for I/O. A single ASIC serves as the interface between the two buses. By including internal read and write buffers, it substantially improves overall performance. In addition, the interface chip includes a separate MMU (TLB and page-table walking hardware) for direct virtual memory accesses (DVMA) performed by I/O devices. In earlier desktop SPARCstation systems the I/O MMU and the CPU's MMU were combined. Dedicated MMUs, enables I/O and the CPU to perform address translation in parallel for different virtual addresses.

In the SPARCstation 10 system, the MSI chip has a separate I/O MMU that is a simplified version of the SRMMU (which is part of the SuperSPARC CPU). The I/O MMU is used to perform address translation whenever an SBus master is granted use of the SBus, including references to system memory on the MBus or when accessing other SBus devices. The I/O MMU is not used for processor references (that is, MBus references) to the SBus, as the MBus is a physically addressed bus, and address translation will already have been performed by the processor's MMU.

SBus Slots and Back Panel

The SPARCstation 10 system supports four SBus slots, in what appears to be the same package as earlier SPARCstation systems. The internal volume of the package has been increased by lowering the bottom of the package and making it flush with the surface of the desktop. This makes it possible to stack two SBus slots on top of each other using a tall and short SBus connectors. The SBus slots provide the means to interface a variety of I/O options, including network interfaces such as FDDI, graphics adapters such as true color frame-buffers and video capture cards, laser printer interfaces, and over 250 third-party SBus cards.

Besides the four SBus slots, there are a variety of standard on-board devices, including:

- Ethernet
- Two ISDN ports
- Two serial-ports
- Parallel port
- Digital audio port
- SCSI
- Keyboard/Mouse

The connectors for these devices are shown in Figure 2-3.

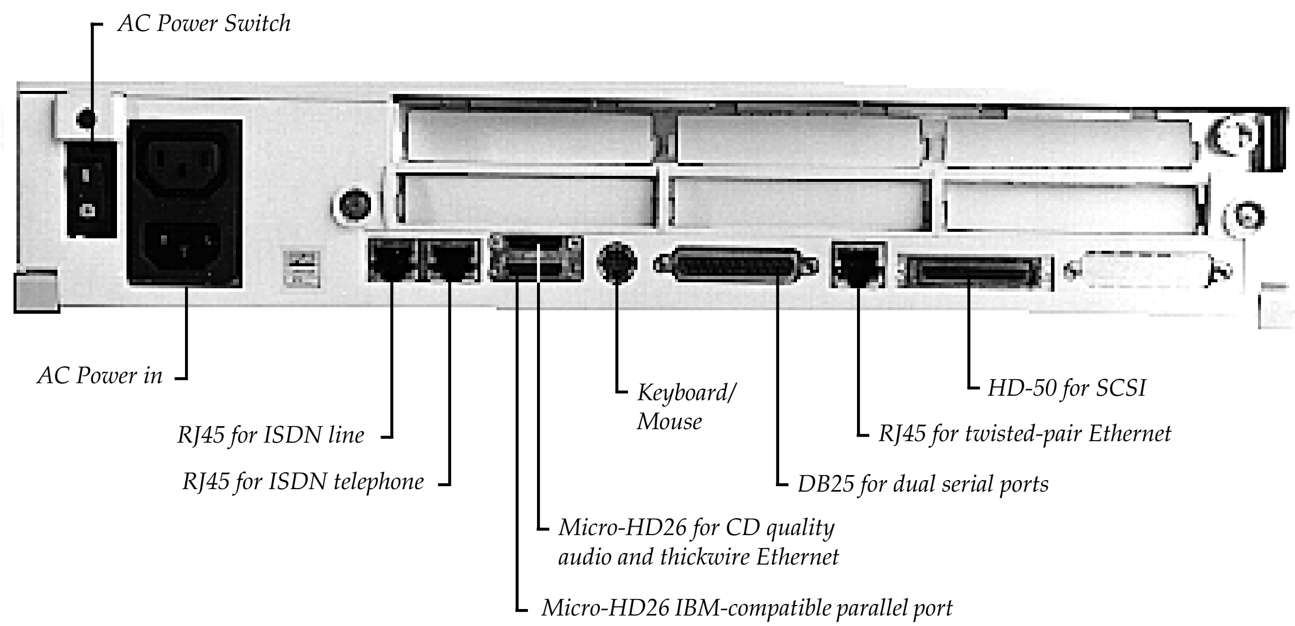


Figure 2-3 SPARCstation 10 system backpanel connectors

Ethernet

Like earlier machines, the SPARCstation 10 system supports standard 10 Mbits per second Ethernet featuring a standard 802.3 interface. However, because of the popularity of twisted-pair Ethernet, and because the RJ45 connector is more reliable and easier to use, the twisted-pair Ethernet connector has replaced the thickwire DB-15 Ethernet connector. Because many installations still use thickwire Ethernet, the SPARCstation 10 system provides access to a thickwire interface via a new micro high-density 26-pin connector (micro-HD26).

Integrated Services Digital Network (ISDN)

ISDN provides an important interface to what is becoming the worldwide standard for wide-area networking and digital telephony. ISDN has a number of benefits beyond normal modems, including higher data rate (144 Mbits per second), a set of OSI compatible protocol layers, and digital access to billing and other telephone services.

The SPARCstation 10 system provides two RJ45 connectors for basic-rate ISDN (BRI). Nominally, one of these connectors plugs into a standard ISDN telephone set (similar to standard digital telephones, except for the interface). The other connects to the telephone jack in the wall, and thus to a PBX or local telephone company.

BRI has somewhat slower bandwidth than primary rate ISDN (PRI) but it is less expensive and somewhat easier to implement. BRI uses two channels (each B channel is 64 Kbytes per second) for data and one D channel (at 16 Kbytes per second) for control.

Applications can use ISDN through the SPARCstation 10 system's ISDN interfaces, for worldwide access through telephone or another computer both to files via protocols such as NFS and to personal data such as voice mail and electronic mail.

Because ISDN provides uncompressed real-time bandwidth of up to 144 Mbits/second, it also enables a number of multimedia applications including worldwide video teleconferencing using compression standards such as H.261 (also known as Px64).

Digital Audio

The SPARCstation 1 system was the one of the first workstations to include audio as a standard feature. This audio was "telephone-quality"; that is, an 8-KHz sampling rate, with 8 bits per sample, μ-law encoded. This quality of audio is adequate for voice attachments to email and other applications that are now standard. However, for multimedia applications, higher quality audio and stereo input and output are necessary.

The SPARCstation 10 system has a threefold solution to audio: First, to provide greater convenience in using audio, a special speaker box is bundled (see Figure 2-4) with every SPARCstation 10 system. A small external microphone can be plugged in making audio input and output more convenient for all applications. Keyboard controls are included for volume control.

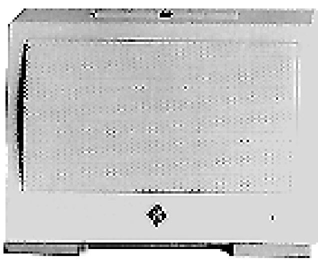


Figure 2-4. The speaker box, which comes standard on SPARCstation 10 configurations, allows for 16-bit CD-quality audio sampling. You can play back voice and music in multi- media applications. Plus you can attach headphones and additional speakers.

A second attribute of the speaker box is that it provides a breakout to a variety of standard phone connectors for those situations where it is necessary to connect the SPARCstation 10 system to standard audio equipment such as amplifiers and tape recorders.

The interface between the speaker box and the SPARCstation 10 system is a digital interface based on a high-speed time-division-multiplexed bus, called CHI. CHI is capable of simultaneous input and output of 16-bit stereo audio at rates up to 48 KHz (the rate used by Digital Audio Tape). All analog components are in the speaker box. This aspect of the design alone improves audio quality by removing a variety of digital noise that is hard to remove in designs where the analog components are on the same board as a high-speed computer. Equally important is a custom single-chip stereo "codec" that supports a a variety of standard sampling rates, including:

- 16-bit 48-KHz Digital Audio Tape
- 16-bit 44.1-KHz CD
- 16-bit, 16-KHz medium-quality audio for applications such as speech processing
- 8-bit μ-law, 8-KHz standard telephony.

Applications can select the appropriate data rate and sample size. For space-sensitive applications such as email, the 8-bit 8-KHz rate is appropriate. For multimedia applications, the 16-bit 44.1-KHz rate may be more appropriate.

Parallel Port

The usefulness of parallel ports on desktop machines has grown due to the increased availability of peripherals that use them, especially low-cost high-quality printers. Using Sun's NeWSprint™ software, a SPARCstation 10 system can directly drive a variety of such printers. In addition, with data rates up to 4 Mbytes per second, the bidirectional parallel port can be used for a variety of other applications such as data acquisition.

The parallel port can operate in programmed I/O mode or be driven by DMA. Its interface direction, timing, and protocol is programmable to meet the wide variety of Centronics interfaces that exist on peripheral devices.

Serial Ports

RS-232 ports provide a convenient way to interface a SPARCstation 10 system to devices such as modems and terminals. Like earlier SPARCstation systems, the SPARCstation 10 system includes two serial ports and like the SPARCstation SLC and SPARCstation ELC systems, it uses a single DB25 and standard ANSI pinout. A single serial port connection can be plugged directly into the machine. If both serial ports are required separately, then the Y cable provided with the system can be used as a breakout to two standard DB25 connectors. When split into two serial ports, serial port A is fully synchronous while serial port B is asynchronous. Synchronous transfers can occur at 56 Kbaud, while asynchronous transfers can occur at up to 19.2 Kbaud.

SCSI

The SPARCstation 10 workstation's fast 8-bit single-ended SCSI interface offers a major improvement over earlier machines by supporting 10 Mbytes/second synchronous transfers, and slower asynchronous SCSI common to last-generation disk drives.

The SPARCstation 10 workstation's new Direct Memory Access controller ASIC (DMA2) provides DMA access to three external interfaces:

- AMD7990 Ethernet controller (LANCE)
- NCR53C90 SCSI controller (ESP)
- Programmable parallel port

The DMA2 chip contains internal buffering for these DMA channels in the form of a 64-byte cache for the LANCE interface and two 64-byte FIFOs for the ESP and parallel port interfaces. The design of the DMA2 is based on the SPARCstation 2 system's S4-DMA+ chip. The DMA2 software is therefore compatible with existing device drivers and SBus cards. In addition, the DMA2 incorporates a number of new features for increasing performance and allowing different modes of operation:

- 10 Mbytes/second SCSI controller transfers

- 1.25 Mbyte/second Ethernet transfers
- 4 Mbytes/second parallel port transfers

Type-5 Keyboard and Mouse

Standard with the SPARCstation 10 system is the new Type-5 keyboard (shown in Figure 2-5), which has a layout compatible with the common IBM AT 101-key keyboard. For UNIX users, a keyboard with a UNIX layout is also available. This new keyboard includes keys for controlling audio and for turning the system on.

Two keyboards are available with the SPARCstation 10 series: an ergonomic, easy-to-use Sun Type-5 keyboard (AT-101 PC-style) and one for traditional UNIX users.

Figure 2-4 New Type-5 Keyboard and Mouse

Graphics and Other Peripherals 3

The SPARCstation 10 system supports a variety of graphics interfaces from Sun and from third-party vendors. As part of the standard configuration, the SPARCstation 10 system includes an 8-bit GX graphics accelerator. Other graphics options include:

- GXplus — Accelerated true color plus double buffering
- GS — Low-cost power 3-D graphics
- GT — Premier graphics for 3-D modeling

Sun's Open Graphics Initiative program encourages third-party suppliers to provide a wide assortment of graphics products (frame buffers, software APIs, and so on) on Sun Workstations.

Software 4

Software

Solaris® 1.1 software (SunOS 4.1.3 operating system and OpenWindows Version 3.0 platform) is pre-installed on the disk of the SPARCstation 10 system. This new version of the operating system and window system are compatible with existing applications.

A new SPARCompiler™ product is available as an independent package. It has a code generator tuned to the SuperSPARC microprocessor's new pipeline. Though most applications will run significantly faster on the SPARCstation 10 system without recompilation, the advance code generator in the SPARCompiler 3.0 product is tuned to give ultimate performance from the machine.

Design and Implementation 5

The SPARCstation 10 system shares a design philosophy first adopted by Sun in the SPARCstation 1 system. Fundamental to this philosophy is the use of state-of-the-art VLSI technology in both the processor and support components, and the use of ASICs wherever possible to reduce parts count and increase performance and reliability. Table 5-1 describes the custom and semi-custom chips designed for the SPARCstation 10 system.

Table 5-1 ASICs and Custom ICs in SPARCstation 10 system

Name	**Description**	**Type**	**Size**	**Package**
EMC	Memory Control	GA[1]	40K Gates	299 PGA
MSI	MBus SBus Interface	GA	40K Gates	223 PGA
DMA2	Ethernet, SCSI, parallel port	GA	30K Gates	160 PQFP
SEC	SBus to 8-bit bus	GA	20K Gates	160 PQFP
SuperSPARC	Superscalar SPARC	FC[2]	3M Transistors	293 PGA
SuperCache	Cache controller	FC	2M Transistors	369 PGA
DBRI	Dual ISDN interface	SC[3]	72K Gates	132 PQFP
MMCodec	Stereo Codec	FC	32K Gates	44 PLCC

1. GA = Gate Array. 2. FC= Full Custom. 3. SC = Standard Cell.

Another aspect of Sun's design philosophy is full system simulation. Before a single chip was fabricated, the entire SPARCstation 10 system CPU board was simulated, including the SuperSPARC processor, all ASICs, and all I/O and peripheral chips. Included as part of this simulation were models for the Ethernet, SCSI disks, and the parallel port. The simulation was performed using Verilog, and was run on a SPARCserver 490.

The four ASICs in the system were implemented using LSI Logic 100K and 200K CMOS logic family. The designs were created using either Verilog or LSI Logic's Less VHDL and then synthesized to gates using the Synopsys design compiler.

Table 5-2 Tools used in designing the SPARCstation 10

Level	Function	Tool
Chip	Gate Array Design Logic Synthesis	LSI Logic MDE LSI Logic Less, Synopsys
	System Simulation	Verlog
Board-Level	Schematic Capture	Valid Logic
	PCB Layout	Valid Logic Allegro
	Timing Verification	Quad Design Motive, Sun Tools
Mechanical	Packaging	Computervision CADDS4X
	Thermal Analysis	FLOMERICS
	Structural Analysis	Stresslab, ANSYS
	Flow Analysis	MOLDFLOW
Management	Scheduling	SunTrac
	Documentation	FrameMaker, Interleaf

SPARCstation 10 Compared to Other Systems 6

Developing a new computer system requires necessary trade-offs to optimize cost, time to market, and competitive position. Designers must choose between various alternatives, using technical information where available, and rely on a variety of metrics which compare and contrast several machines.

Six machines were compared: the SPARCstation 10 system, the HP 720 and 730, the IBM 340 and 350, and the DEC 5000/240. These machines loosely represent a set from which a customer might actually need to choose while simultaneously providing a fair example of each company's desktop technology.

Table 6-1 Comparison of Package Sizes

Dimension	**SPARCstation 10**	**HP 720**	**HP 730**	**IBM 340**	**IBM 350**	**DEC 5000/240**
Height	3 in.	4.5 in.	4.5 in.	6.4 in.	6.4 in.	3.6 in.
Width	16.3 in.	20 in.	20 in.	18 in.	18 in.	20.1 in.
Depth	16.1 in.	17.5 in.	17.5 in.	20.6 in.	20.6 in.	17.1 in.
Footprint [1]	262 in.	350 in.	350 in.	371 in.	371 in.	344 in.
Volume[2]	787 in.	1575 in.	1575 in.	2373 in.	2373 in.	1237 in.

1. In square inches.
2. In cubic inches.

Four of the six machines meet the "desktop" criterion—namely, when placed on top of the CPU box, the monitor is at a comfortable reading height. Because space is often limited, being able to hide the CPU under the monitor is an important product feature.

All systems come with internal disk storage supporting 2 3.5 in. disk drives. Only the SPARCstation 10 comes with a floppy drive standard. The ability to tailor a machine to individual requirements is important to end users. With the exception of the HP systems, all machines provide several expansion slots via which users can add various expansion options.

All the systems provide 5 Mbytes per second SCSI except the SPARCstation 10 system, which provides double the SCSI performance operating at 10 Mbytes per second.

The SPARCstation 10 system is the first machine to incorporate ISDN as a standard feature on the motherboard. It also offers 16-bit CD-quality audio, HP and DEC machines offer 8-bit audio, and IBM supports none.

Table 6-2 Comparison of Workstation Features of the SPARCstation 10 system

Feature	**SPARCstation 10**	**HP 720**	**HP 730**	**IBM 340**	**IBM 350**	**DEC 5000/240**
Disks	2 x 3.5 in.	2 x 3.5 in.	2 x 3.5 in.	2 x 3.5 in.	2 x 3.5 in.	N/A
Floppy	1 standard	1 optional[1]	1 optional[1]	1 optional	1 optional	N/A
Expansion Slots	4	1 optional	1	4	4	3
Bus Type	SBus	EISA	EISA	MicroChannel	MicroChannel	Turbochannel
SIMMs	512 Mbytes	128 Mbytes	128 Mbytes	128 Mbytes	128 Mbytes	480 Mbytes
Ethernet ISDN	AUI, 10BaseT Yes	AUI No	AUI No	Thick/Thin No	Thick/Thin No	Thick No
SCSI	10 Mbytes/sec	5 Mbytes/sec	5 Mbytes/sec	5 Mbytes/sec	5 Mbytes/sec	5 Mbytes/sec
Audio	16-bit	8-bit	8-bit	None	None	8-bit
Power Supply	140 W	200 W	200 W	265 W	265 W	359 W
Processor	SuperSPARC	HP-PA 1.1	HP-PA 1.1	POWER	POWER	R4000
Clock Frequency	36-45 MHz	50 MHz	66 MHz	33 MHz	42 MHz	40 MHz
Onchip Cache D/I External Cache	16/20 KB, 1 MB external	None 256/128 KB	None 256/128 KB	None 32/8 KB	None 32/8 KB	None 64/64 KB

1. Requires one disk slot.

Table 6-3 Some performance comparisons.[1]

Feature	SPARCstation 10	HP 720	HP 730	IBM 340	IBM 350	DEC 5000/240
SPECint92	44.2, 52.6[2]	36.4	48.1	27.7	34.6	N/A
SPECfp92	52.9, 64.7[2]	58.2	75.0	51.9	65.0	N/A
SPECthruput89	109, 218[3]	N/A	N/A	N/A	N/A	N/A
MIPS	86.1, 96.2, 200+[4], 400+[4]	57.9	76.7	N/A	77.2	42.9
MFLOPS	10.6, 17.2, 38[4], 76[4]	17.9	23.7	14.8	18.6	6.0

1. Solaris 1.1, and a combination of Apogee/KAP and SunPro/KAP compilers. 2. SPEC92 numbers for the Model 30 and Model 41. 3. No MP SPEC92 definition exists at this time for multiprocessors so SPECthruput89 estimates are provided for the Model 52 and Model 54. 4. MP system performance numbers are estimates.

Conclusions

The SPARCstation 10 system demonstrates how SPARC technology continues to scale to higher performance and new system architectures. Compared to the SPARCstation 1 system, the SPARCstation 10 system is over four times faster as a uniprocessor and is more than twice as fast as the SPARCstation 2 system. The SPARCstation 10 system is the first high-volume desktop symmetric multiprocessor workstation, which provides additional means to extend the performance of the system.

Equally important are new systems features incorporated in the SPARCstation 10 system, including ISDN, up to 512 Mbytes of ECC Memory, four SBus slots, and field upgradable processor modules.

As a result, the SPARCstation 10 system is ideally positioned to take advantage of the more than 4,000 existing SPARC solutions while offering significant new functionality to support next-generation network, telephony, and multimedia applications.

SPARCstation 10 Specifications

A

	Model 30	*Model 41*	*Model 52*	*Model 54*
Number of Processors	One	One	Two	Four
On-chip cache	36 KB	36 KB	2 x 36 KB	4 x 36 KB
SuperCache	None	1 MB	2 x 1 MB	4 x 1 MB

Processor

Architecture	Superscalar SPARC Version 8
Memory management	SPARC reference MMU with 65,536 contexts
	Primary: 20-KB instruction, and 16-KB data on-chip
	Secondary: 1-MB external optional
CPU interface	Two 64-bit MBus slots for multiprocessing

Main Memory

16- and 64-MB SIMM expansion
128 MB maximum (with 16-MB SIMMs)
512 MB maximum (with 64-MB SIMMs)

Standard Interfaces

Ethernet Type	10-Mb/sec twisted pair standard (10BaseT)
	AUI available with optional adapter cable
SCSI	10-MB/sec SCSI-2 (synchronous)
Serial	Two RS-232C/RS-423 serial port
Parallel	Centronics-compatible parallel port
Audio	CD-quality 16-bit audio, 8 to 48 KHz
	External speaker box and microphone
ISDN	Dual basic-rate (2B+D) interface; 144 Kb/sec
SBus	Four expansion slots; 32-bit data bus width

Mass Storage

Floppy disk	3.5 in. MS-DOS/IBM® compatible (720 KB, 1.2 MB, 1.44 MB formatted)
Internal disk	Up to two 3.5-in. disks (424 MB or 1 GB formatted)
External desktop storage	Disk: 424 MB 3.5 in.; 1.3 GB 5.25 in.; 644-MB CD-ROM Tape: 150-MB .25-in. QIC-150; 5 GB 8 mm

Graphics Options

SPARCstation 10GX	8-bit 2-D/3-D wireframe, 1152 x 900 resolution
SPARCstation 10GXplus	8-bit 2-D/3-D wireframe, 1280 x 1024 resolution, hardware double buffering
SPARCstation 10GS	24-bit 3-D solids, 1152 x 900 resolution, double buffering, Z-buffer, Gouraud shading, depth cueing
SPARCstation 10GT	24-bit 3-D solids, 1280 x 1024 resolution, Z-buffer, Gouraud shading, depth cueing, transparency, anti-aliasing, overlays

Monitor Options

16-in. color	1152 x 900 resolution, 76- or 66-Hz refresh rate, 100 dots per inch
19-in. color	1152 x 900 resolution, 76- or 66-Hz refresh rate, 84 dots per inch 1280 x 1024 resolution, 67-Hz refresh rate, 93 dots per inch (GXplus)
21-in. color	1152 x 900 resolution, 76-Hz refresh rate, 87 dots per inch
19-in. grayscale	1152 x 900 resolution, 76-Hz refresh rate, 84 dots per inch

Input Devices

Keyboard	Sun Type-5, AT 101 or UNIX layout available More than 18 international keyboards available
Mouse	Optical, 3-button

Software

Operating system	Solaris 1.1 SMCC Version A
Window system	OpenWindows Version 3
Languages	C, C++, Pascal, FORTRAN
Networking	ONC, NFS®, TCP/IP, SunNet™, OSI, MHS
Graphics	SunVision™, SunPHIGS™, XGL™, SunGKS™, Xlib, PostScript®

Environment

AC power	100-240 VAC, 47-63 Hz, 0.4 K VA
Operating	0° C to 40° C (32° F to 104° F)
	5% to 95% relative humidity, noncondensing
Nonoperating	-40° C to 75° C (-40° F to 167° F)
	5% to 95% relative humidity, noncondensing
Operating acoustic noise	5.1 bels (at 28° C)
Idle acoustic noise	5.0 bels (at 28° C)

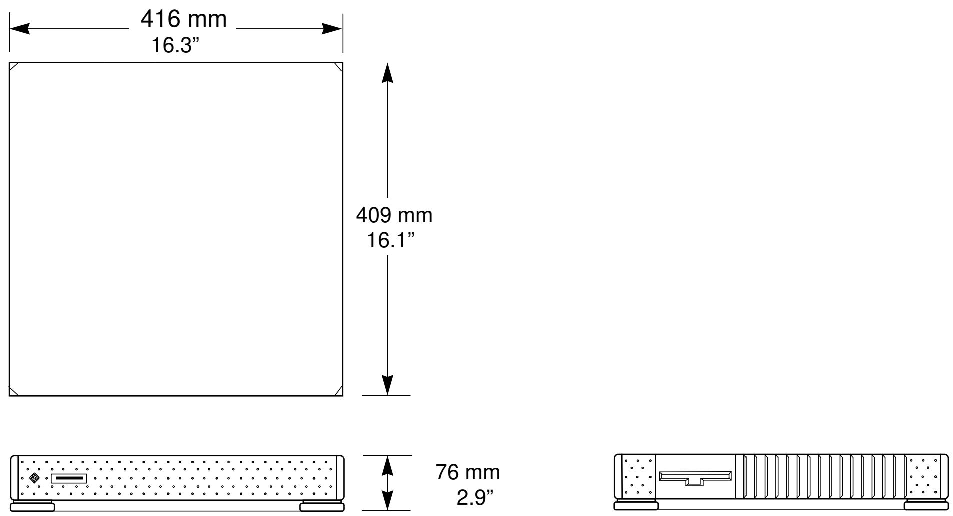
Declared noise emissions in accordance with ISO 9296

Regulations

Meets or exceeds the following requirements:

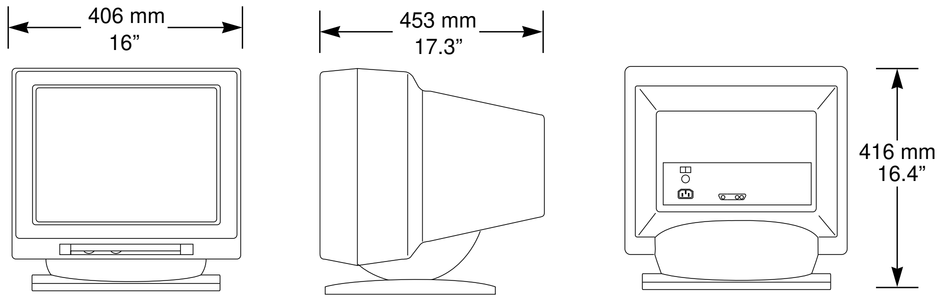
Safety	UL 1950, CSA 950, TUV EN 60950
RFI/EMI	FCC Class B, DOC Class B, VDE Class B, VCCI Class 2
X-ray	DHHS 21, Subchapter J, PTB German X-ray Decree

Dimensions and Weights

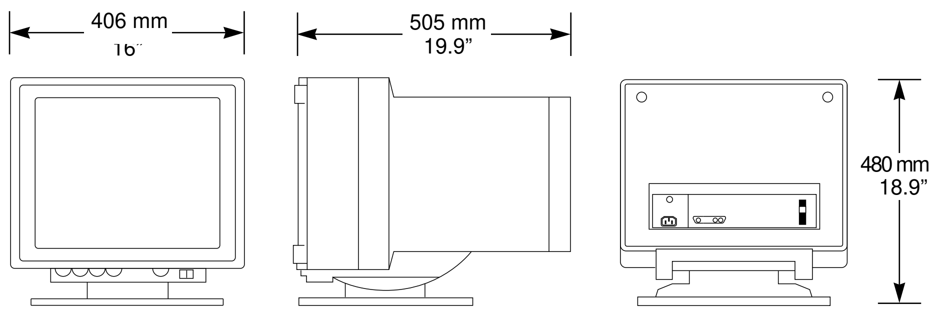


SPARCstation 10 Chassis

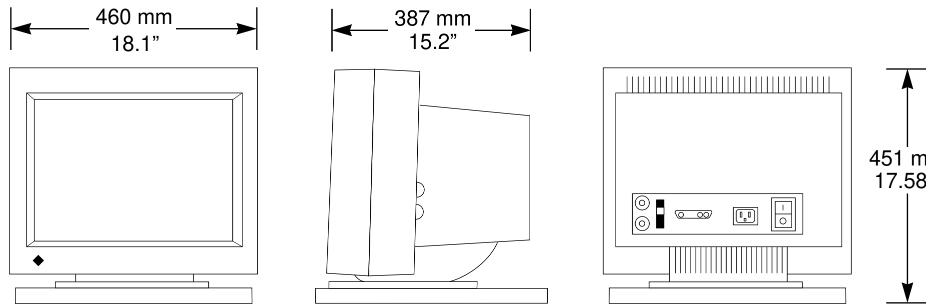
Height	7.6 cm (3.0 in.)
Width	41.7 cm (16.4 in.)
Depth	40.9 cm (16.1 in.)
Shipping weight	12.7 kg (27.0 lbs.)



16-in. color	
Height	41.6 cm (16.4 in.)
Width	40.6 cm (16.0 in.)
Depth	45.3 cm (17.8 in.)
Shipping weight	27.3 kg (60.0 lbs.)



19-in color	
Height	47.4 cm (18.7 in.)
Width	48 cm (18.9 in.)
Depth	50.5 cm (19.9 in.)
Shipping weight	38.6 kg (85.0 lbs.)



19-in. grayscale

Height	45.0 cm (17.7 in.)
Width	46.0 cm (18.1 in.)
Depth	41.o cm (16.1 in.)
Shipping weight	27.7 kg (61.0 lbs.)

Upgrades

Upgrades are available for the SPARCstation 1, SPARCstation 1+, SPARCstation IPX, SPARCstation 2, and Sun-3™ systems.

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